

Form PTO-1449 (modified)
INFORMATION DISCLOSURE CITATION

Atty. Docket No.

Serial No.

1138-71

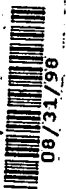
Applicant:
Tsang et al.

Filing Date

Group

Sheet 1 of 1

JCS11 U.S. PTO
09/144579



U.S. Patent Documents

Examiner Initial	Document Number	Date	Name
------------------	-----------------	------	------

Foreign Patent Documents

Other Documents (including Author, Title, Date, Pertinent Pages)

Loke

Baba, Y., et al, "A Study on a High Blocking Voltage UMOS-FET With a Double Gate Structure," Proceedings of 1992 International Symposium on Power Semiconductor Devices & ICs, Institute of Electrical Engineers of Japan and IEEE Electron Devices Society, Toyko, Japan, pp. 300-302.

Examiner.

Loke

Date Considered

5/2/00

*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (modified)
INFORMATION DISCLOSURE CITATION

Atty. Docket No.
1138-71

Serial No.

Applicant:
Tsang et al.

Filing Date

Group

Loke

H. R. Chang, B. J. Baliga, J.W. Kretchmer, and P.A. Placente, "Insulated Gate Bipolar Transistor (IGBT) with a Trench Gate Structure," IEEE IEDM Tech. Digest, pp. 674-677, 1987.

S. Mukherjee, M. Kim, L. Tsou, and M. Simpson, "TDMOS- An Ultra-Low On-Resistance Power Transistor," IEEE Trans. Electron Dev. ED-35, No. 12, p. 2459, Dec. 1988.

C. Bulucea, M. R. Kump, and K. Amberiadis, "Field Distribution and Avalanche Breakdown of Trench MOS Capacitor Operated in Deep Depletion," IEEE Trans. Electron Dev. ED-36, No. 11, pp. 2521-2529, Nov. 1989.

K. Shenai, "Optimally Scaled Low-Voltage Vertical Power MOSFET's for High-Frequency Power Conversation, IEEE Trans. Electron Dev. Vol. 37, No. 4, April 1990.

K. Shenai, W. Hennessy, M. Ghezzi, D. Korman, H. Chang, V. Temple, and M. Adler, "Optimum Low-Voltage Silicon Power Switches Fabricated Using Scaled Trench MOS Technologies," IEEE IEDM Tech. Digest pp. 793-797, 1991.

K. Shenai, "A 55-V, 0.2-mΩ-cm² Vertical Trench Power MOSFET," IEEE Electron Dev. Lett. EDL-12, No. 3, pp. 108-110, Mar. 1991.

Loke

S. Matsumoto, T. Ohno, K. Izumi, "Ultralow Specific on Resistance Umosfet with Trench Contacts for Source and Body Regions Realised By Selfaligned Process," Electronics Letters, Vol. 27, No. 18, pp. 1640-1641, August 29, 1991.

Examiner

Loke

Date Considered

5/2/00

*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (modified)
INFORMATION DISCLOSURE CITATION

Atty. Docket No.

Serial No.

1138-71

Applicant:
Tsang et al.

Filing Date

Group

JCS11 U.S. PTO
09/144579
08/31/98

U.S. Patent Documents

Examiner Initial	Document Number	Date	Name
<u>Loke</u>	4,967,245	10/30/90	Cogan et al.

Foreign Patent Documents

<u>Loke</u>	DE -A-41 11046 A 1	Germany	Nissan Motor
<u>Loke</u>	EP-A-0 342 952	EPO	Advanced Power Technology
<u>Loke</u>	JP-A-01 198076	Japan	Mitsubishi Electric Corp.

Other Documents (including Author, Title, Date, Pertinent Pages)

<u>Loke</u>	Matsumoto, S., et al., "Ultralow Specific on Resistance UMOSFET with Trench Contacts for Source and Body Regions Realised by Selfaligned Process," Electronics Letters, 29 Aug. 1991, UK, vol. 27, no. 18, ISN 0013-5194, pages 1640-1642, XPOOO264480
-------------	--

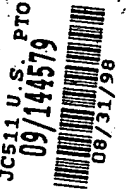
Examiner

Loke

Date Considered

5/2/00

*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



Form PTO-1449 (modified) INFORMATION DISCLOSURE CITATION	Atty. Docket No. 1138-71	Serial No.
Applicant: Tsang et al.		
Filing Date	Group	

U.S. Patent Documents

Examiner Initial	Document Number	Date	Name
<u>Loke</u>	4,070,690	01/24/78	Wickstrom
<u>Loke</u>	4,145,703	03/20/79	Blanchard et al.
<u>Loke</u>	4,994,871	02/19/91	Chang et al.

Foreign Patent Documents

Other Documents (including Author, Title, Date, Pertinent Pages)

Loke

D. Ueda, H. Takagi, and G. Kano, "A New Vertical Power MOSFET Structure with Extremely Reduced On-Resistance," IEEE Trans. Electron Dev. ED-32, No. 1, pp. 2-6, Jan 1985.

D. Ueda, H. Takagi, and G. Kano, "Deep-Trench Power MOSFET with An Ron Area Product of 160 mΩ-mm²," IEEE IEDM Tech. Digest, pp. 638-641, 1986.

H.R. Chang, R.D. Black, V.A.K. Temple, W. Tantraporn and B.J. Baliga, "Ultra Low Specific On-Resistance UMOS FET," IEEE IEDM, pp. 642-645, 1986.

D. Ueda, H. Tagaki, and G. Kano, "An Ultra-Low On-Resistance Power MOSFET Fabricated by Using a Fully Self-Aligned Process," IEEE Trans. Electron Dev. ED-34, No. 4, pp. 926-930, Apr. 1987.

Loke

H. R. Chang, R. D. Black, V. A. K. Temple, W. Tantraporn, and B. J. Baliga, "Self-Aligned UMOSFET's with a Specific On-Resistance of 1 mΩ-cm²," IEEE Trans. Electron Dev. ED-34, No. 11, pp. 2329-2334, Nov. 1987.

Examiner	<u>Loke</u>	Date Considered	<u>5/2/00</u>
----------	-------------	-----------------	---------------

*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.